

VLSI Design
EE465
Fall 2010

- I. Course Number:** EE 465
- II. Course Title:** VLSI Design
- III. Semester Credit Hours:** 3
- IV. Course Description:** This course will cover basic theory and techniques of digital VLSI (Very-Large-Scale Integrated) design in CMOS technology. It will discuss the bottom-up as well as the top-down approach. It will prepare students to design and analyze digital circuits and show them how these circuits are implemented on a VLSI chip. Prerequisite: EE321(Digital Logic)
- V. Required Textbook:** *Introduction to VLSI Circuits and Systems*, John P. Uyemura, Prentice-Hall, 2002, ISBN 0-471-12704-3.
- VI. Student Learner Outcomes:** Upon completion of the course students will :
1. be able to evaluate the effects of transistor characteristics on CMOS circuit performance
 2. be able to take transistor characteristics into consideration when analyzing or designing a CMOS logic circuit
 3. be able to create a circuit schematic from a mask layout
 4. have the knowledge of how to design logic circuits using different logic styles (pass-gate, ratioed logic, dynamic logic)
- VII. Course Outline:** Basic CMOS Logic, Fabrication and layout, Combinational logic design, Sequential logic design, Subsystem Design, Design methodologies
- VIII. Course Requirements:** Attendance of lectures and completion of assignments
- IX. Methods of Evaluation:**
- | | |
|----------|--------|
| Homework | 15 pts |
| Test I | 25 pts |
| Test II | 30 pts |
| Test III | 30 pts |
- X. Grading Scale:** A (100-90), B (89-80), C (79-70), D (69-60), F (59-0)
- XI. Faculty Office Location and Office hours**
- Office: 104D
The instructor can be contacted during the following office hours; other times by appointment only:
Monday: 9am-12pm, 2pm-3pm
Tuesday: 9am-11am, 4pm-5pm
Wednesday: 9am-12pm
- XII. Course Schedule:**
- Topics:**
- | | |
|------------------|---------------|
| Overview of VLSI | week 1 |
| Basic CMOS Logic | weeks 2 and 3 |

Physical structure of CMOS circuits	weeks 4 and 5
Test I	week 6
Physical design	week 7
DC characteristics of CMOS gates	week 8
Advanced techniques in CMOS circuits	weeks 9 and 10
Test II	week 11
VLSI system components	weeks 12 and 13
Arithmetic circuits	week 14
VLSI clocking	week 15
Test III	week 16

XIII. Student Participation:

a. Participation Policy: Students are expected to attend the lectures

XIV. Disability Accommodations: Students with disabilities may request reasonable accommodations through the A&M-Texarkana Disability Services Office by calling 903-223-3062.

XV. Academic Integrity: Academic honesty is expected of students enrolled in this course. Cheating on examinations, unauthorized collaboration, falsification of research data, plagiarism, and undocumented use of materials from any source constitute academic dishonesty and may be grounds for a grade of 'F' in the course and/or disciplinary actions. For additional information, see the university catalog.

XVI. Statement on email usage: Upon application to Texas A&M University-Texarkana an individual will be assigned an A&M-Texarkana email account. This email account will be used to deliver official university correspondence. Each individual is responsible for information sent and received via the university email account and is expected to check the official A&M-Texarkana email account on a frequent and consistent basis. Faculty and students are required to utilize the university email account when communicating about coursework.

XVII. ABET Outcomes Coverage

- (a) an ability to apply knowledge of mathematics, science, and engineering
- (b) an ability to design and conduct experiments, as well as to analyze and interpret data.
- (c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability
- (e) identify, formulate and solve engineering problems
- (i) a recognition of the need for, and an ability to engage in life-long learning
- (k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.