EE 455 – Digital Circuit Testing & Testability

Credits and Contact Hours: 3 credits (One 2hr and 45 minute lecture per week)

Instructor: Parag K. Lala Ph.D.

Faulty Office location and Contact Policy: Dr. Lala’s office 104D, Office hours will be posted at the beginning of the semester

• Other supplemental materials: none

Course Description:

• The complexity of digital circuits placed on IC (Integrated Circuit) chips has significant impact on the cost of testing such chips. Testing is performed to ensure that function/performance have not been altered during fabrication. This course introduces current testing techniques for digital circuits, and design strategies used to enhance their testability.
• Prerequisite: EE320/CS31

• Corequisite: None

• Required, Elective: Required

Course Learning Objectives: By the completion of this course, the student will be able to

1. Apply currently available techniques to derive test patterns/sequences for combinational and sequential circuits
2. Design combinational circuits that are testable.
3. Design testable state machines
4. Apply built-in test features to enhance testability of complex digital circuits

Topics Covered:

Overview of testing, Types of tests, Test Applications (Weeks 1 and 2)

Stuck-at faults, Fault lists, Bridging faults, Transistor faults (Weeks 3 and 4)

Test I

Design representation, Basic concepts of test generation Week 6

D-Algorithm Week 7

PODEM and FAN algorithms Week 8
Design of Testable combinational circuits                           Weeks 9
Test II                                                                 Week 10
Testable state machine design                                        Weeks 11, 12 and 13
Built-in self test techniques                                        Weeks 14 and 15
Test III                                                               Week 16

Evaluation Methods:

   Homework          10 pts
   Test I            30 pts
   Test II           30 pts
   Final Test        30 pts

Grading Scale: A (100- 90), B (89- 80), C (79-70), D (69-60), F (59-0)

ABET Outcome Coverage:

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<tr>
<th>Outcome-related course learning objective</th>
<th>MAPPING among course learning-objectives and ABET student learning outcomes</th>
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<tbody>
<tr>
<td>(i) Apply currently available techniques to derive test patterns/sequences for combinational and sequential circuits</td>
<td>ABET 3b</td>
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<tr>
<td>(ii) Design combinational circuits that are testable</td>
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<td>(iii) Design testable state machines</td>
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(iv) Apply built-in test features to enhance testability of complex digital circuits

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<td>Test 3</td>
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**Disability Accommodation**

Students with disabilities may request reasonable accommodations. Nikki Thomson (alternate) 903-223-3083 nikki.thomson@tamut.edu

**Academic Integrity**

Academic honesty is expected of students enrolled in this course. Cheating on examinations, unauthorized collaboration, falsification of research data, plagiarism, and undocumented use of materials from any source, constitute academic dishonesty, and may be grounds for a grade of "F" in the course and/or disciplinary actions." For additional information see the university policy manual.

**Statement on email usage**

Upon application to Texas A&M University-Texarkana an individual will be assigned an A&M-Texarkana email account. This email account will be used to deliver official university correspondence. Each individual is responsible for information sent and received via the university email account and is expected to check the official A&M-Texarkana email account on a frequent and consistent basis. Faculty and students are required to utilize the university email account when communicating about coursework.

**Drop Policy:**

University Drop Policy: To drop this course after the 12th class day, a student must complete the Drop/Withdrawal Request Form, located on the University website http://tamut.edu/Registrar/droppingwithdrawing-from-classes.html) or obtained in the Registrar's Office. The student must submit the signed and completed form to the instructor of each course indicated on the form to be dropped for his/her signature. The signature is not an "approval" to drop, but rather confirmation that the student has discussed the drop/withdrawal with the faculty member. The form must be submitted to the Registrar's office for processing in person, email Registrar@tamut.edu, mail (P. O. Box 5518, Texarkana, TX 75505) or fax (903-223-3140). Drop/withdraw forms missing any of the required information will not be accepted by the Registrar's Office for processing. It is the student's responsibility to ensure that the form is completed properly before submission. If a student stops participating in class (attending and submitting assignments) but does not complete and submit the drop/withdrawal form, a final grade based on work completed as outlined in the syllabus will be assigned.