EE 455 – Digital Circuit Testing & Testability

Credits and Contact Hours: 3 credits (One 2hr and 45 minute lecture per week)

Instructor: Parag K. Lala Ph.D.

Textbook: Samiha Mourad and Yervant Zorian, Principles of Testing Electronic Systems, First Edition, John Wiley Science, 2000

- Other supplemental materials: none

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Course Description:

- Catalog Description: The complexity of digital circuits placed on IC (Integrated Circuit) chips has significant impact on the cost of testing such chips. Testing is performed to ensure that function/performance have not been altered during fabrication. This course introduces current testing techniques for digital circuits, and design strategies used to enhance their testability.
- Prerequisite: EE320/ CS321
- Corequisite: None
- Required, Elective: Required

Course Learning Objectives: By the completion of this course, the student will be able to

1. Apply currntly available techniques to derive test patterns/sequences for combinational and sequential circuits
2. Design combinational circuits that are testable.
3. Design testable state machines
4. Apply built-in test features to enhance testability of complex digital circuits

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Topics Covered:

Overview of testing, Types of tests, Test Applications	(Weeks 1 and 2)
Stuck-at faults, Fault lists, Bridging faults, Transistor faults	(Weeks 3 and 4)
Test I	Week 5
Design representation, Basic concepts of test generation	Week 6
D-Algorithm	Week 7
PODEM and FAN algorithms	Week 8
Design of Tesstable combinational circuits	Weeks 9
Test II	Week 10

Testable state machine design	Weeks 11, 12 and 13
Built-in self test techniques	Weeks 14 and 15
Test III	Week 16

Evaluation Methods:

Homework	10 pts
Test I	30 pts
Test II	30 pts
Final Test	30 pts

Grading Scale: A (100- 90), B (89- 80), C (79-70), D (69-60), F (59-0)

ABET Outcome Coverage:

MAPPING among course learning-objectives and ABET student learning outcomes				
Outcome-related course learning objective	**ABET 3b**	**ABET 3c**	**ABET 3e**	**ABET 3i**
(i) Apply currntly available techniques to derive test patterns/sequences for combinational and sequential circuits	2 **Test 1**			
(ii) Design combinational circuits that are testable			2 Test 2	
(iii) Design testable state machines		2 Homework t		2 **Test 3**

(iv) Apply built-in test features to enhance testability of complex digital circuits .			3 Test 3	